Amendment to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.   (Currently amended) An apparatus comprising:

a ~~storage block~~memory configured to store a thread switching structure;

an execution block configured to execute instructions; and

a thread management block coupled to the storage and execution blocks, the thread management block equipped to maintain the thread switching structure in the storage block to facilitate interleaving execution of a plurality of threads of instructions by the execution block, with the thread switching structure including a current thread identifier identifying one of the plurality of threads as a current thread being currently executed by the execution block, and a thread array of thread entries, one per thread, ~~correspondingly~~ describing ~~the plurality of threads~~ at least a plurality of registers of an external set of registers, on which the corresponding described thread depends, each thread entry being created and added to the thread array by the thread management block as part of the execution of a create thread instruction of a thread to spawn execution of another thread, and wherein the thread management block is further equipped to select a non-current one of the plurality of threads to be the new current thread to be executed on one of a round-robin basis, a fixed priority basis, or a rotating priority basis and switch execution to a first instruction of the new current thread as part of a thread switching instruction of a thread to instruct the execution block to switch execution to another thread.

2.   (Previously presented) The apparatus of claim 1, wherein each thread entry comprises a thread program counter to identify an instruction of the corresponding described thread as a current instruction to be executed, when the corresponding described thread is being executed.

3.   (Previously presented) The apparatus of claim 1, wherein each thread entry comprises an activeness indicator indicating whether the corresponding described thread is currently in an

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active state or an inactive state, where the corresponding described thread is to be included among the threads to be interleavingly executed by the execution sub-block, while the thread is in the active state, and not included, while the thread is in the inactive state.

4.   (Previously presented) The apparatus of claim 3, wherein the thread management block is equipped to reset the activeness indicator of a thread from the active state to the inactive state, as part of the execution of a thread termination instruction of a thread terminating its own execution.

5.   (Canceled)

6.   (Previously presented) The apparatus of claim 1, wherein the input/output interface is configured to couple the apparatus to an external set of registers.

7.   (Canceled)

8.   (Canceled)

9.   (Previously presented) The apparatus of claim 1, wherein the processing block further comprises an input/output interface configurable to be a selected one of an input interface and an output interface to particularize the processing block as a selected one of an input processing block and an output processing block of a signal processing macroblock.

10.   (Previously presented) The apparatus of claim 1, further comprising another storage block coupled to the execution block, to store instructions of the threads.

11.   (Currently amended) A method comprising:
        fetching a first instruction of a first thread of instructions; and
        executing, via an execution sub-block, the first instruction, and as part of the execution of the first instruction, adding a first thread entry in a thread array of a thread switching structure, wherein the first thread entry comprises thread dependency information describing at least a

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plurality of registers of an external set of registers, on which the first thread depends, if the first instruction is a create thread instruction spawning interleaved execution of a second thread of instructions with execution of other threads, and selecting the second thread from among a plurality of active threads, updating the current thread identifier to identify the second thread as a new current thread to be executed, replacing the first thread, and transferring execution to an instruction of the second thread instead, if the first instruction is a thread execution switching instruction, and execution of the second thread has previously been spawned, the thread switching structure being disposed and maintained within a ~~storage sub-block~~memory by a thread management sub-block to facilitate interleaved execution of threads of instructions by the execution sub-block, and the first thread entry describing the second thread.

12.   (Original) The method of claim 11, wherein the first thread entry comprises a thread program counter to identify an instruction of the second thread as a current instruction to be executed, when the second thread is being executed.

13.   (Original) The method of claim 11, wherein the first thread entry comprises an activeness indicator indicating whether the second thread is currently in an active state or an inactive state, where the second thread is to be included among the threads to be interleavingly executed, while the second thread is in the active state, and not included, while the second thread is in the inactive state.

14.   (Canceled)

15.   (Original) The method of claim 11, wherein said execution of the first instruction includes resetting an activeness indicator of a second thread entry of the thread array from indicating an active state to indicating an inactive state instead, if the first instruction is a thread termination instruction terminating execution of the first thread, the second thread entry being corresponding to the first thread.

16.   (Canceled)

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17.   (Original) The method of claim 16, wherein said selection of the second thread from among a plurality of active threads comprises selecting the second thread in a selected one of a round-robin basis, a fixed priority basis, and a rotating priority basis.

18.   (Currently amended) A signal processing macroblock comprising:

a set of registers; and

at least a selected one of

an input processing block coupled to the set of registers, including an input interface, execution and thread management facilities equipped to support interleaved execution of multiple threads of instructions, the thread management facilities including a thread management sub-block equipped to maintain a thread switching structure <u>including a current thread identifier to identify one of the plurality of threads as a thread to be executed, and a thread array of</u> ~~and create and add~~ thread entries<u>, one per thread, configured to describe the set of registers on which the</u> corresponding <u>threads depend, each thread entry to be created and added to the thread array by the thread management sub-block based on a create thread instruction</u>~~to the multiple threads of instructions to a thread array within the thread switching structure~~<u>, and wherein the thread management sub-block is further configured to select another thread of the plurality of threads to be executed based on a thread switching instruction, wherein the thread switching instruction may select a thread based on a fixed priority basis, a round robin basis, or a rotating priority basis</u>; and

an output processing block coupled to the set of registers, including an output interface, execution and thread management facilities equipped to support interleaved execution of multiple threads of instructions, the thread management facilities including a thread management sub-block equipped to maintain a thread switching structure and create and add thread entries corresponding to the multiple threads of instructions to a thread array within the thread switching structure.

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19.   (Original) The signal processing macroblock of claim 18, wherein the signal processing macroblock further comprises a computation block coupled to the set of registers, including execution and thread management facilitates equipped to support interleaved execution of multiple threads of instructions, including instructions performing mathematical operations.

20.   (Original) The signal processing macroblock of claim 19, wherein at least a selected one of the facilities of the input processing block, the output processing block and the computation block, equipped to support interleaved execution of multiple threads, includes a storage sub-block to store a thread switching structure that includes a current thread identifier identifying one of the multiple threads as a current thread to be executed, and a thread array including thread entries describing corresponding ones of the multiple threads.

21.   (Original) The signal processing macroblock of claim 20, wherein at least a selected one of the facilities of the input processing block, the output processing block and the computation block, equipped to support interleaved execution of multiple threads, further includes an execution sub-block equipped to create a thread entry in the thread array for a thread as part of the execution of a create thread instruction spawning interleaved execution of the thread.

22.   (Original) The signal processing macroblock of claim 20, wherein at least a selected one of the facilities of the input processing block, the output processing block and the computation block, equipped to support interleaved execution of multiple threads, further includes an execution sub-block equipped to reset an activeness indicator of a thread entry in the thread array for a thread from indicating an active state to indicating an inactive state as part of the execution of a thread termination instruction terminating execution of the thread.

23.   (Original) The signal processing macroblock of claim 20, wherein at least a selected one of the facilities of the input processing block, the output processing block and the computation block, equipped to support interleaved execution of multiple threads, further includes an execution sub-block equipped to select a thread as a new current thread to be executed, updating a current thread identifier of the thread switching structure to identify the selected thread, and

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switching to execute an instruction of the selected thread, as part of the execution of a thread execution switching instruction.

24.   (Currently amended) A media processor comprising:

a direct memory access unit to access media data;

a plurality of signal processing units coupled to the direct memory access unit to process the accessed media data, at least a first of which signal processing units comprising

a set of registers,

an input processing block coupled to the set of registers, including an input interface, execution and thread management facilities equipped to support interleaved execution of multiple threads of instructions, the thread management facilities including a thread management sub-block equipped to maintain a thread switching structure including a current thread identifier to identify one of the plurality of threads as a thread to be executed, and a thread array of ~~and create and add~~ thread entries, one per thread, configured to describe the set of registers on which the corresponding threads depend, each thread entry to be created and added to the thread array by the thread management sub-block based on a create thread instruction~~to the multiple threads of instructions to a thread array within the thread switching structure~~, and wherein the thread management sub-block is further configured to select another thread of the plurality of threads to be executed based on a thread switching instruction, wherein the thread switching instruction may select a thread based on a fixed priority basis, a round robin basis, or a rotating priority basis; and

an output processing block coupled to the set of registers, including an output interface, execution and thread management facilities equipped to support interleaved execution of multiple threads of instructions, the thread management facilities including a thread management sub-block equipped to maintain a thread switching structure and create and add thread entries corresponding to the multiple threads of instructions to a thread array within the thread switching structure.

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25.   (Original) The media processor of claim 24, wherein the first signal processing unit further comprises a computation block coupled to the set of registers, including execution and thread management facilitates equipped to support interleaved execution of multiple threads of instructions, including instructions performing mathematical operations.

26.   (Original) The media processor of claim 25, wherein at least a selected one of the facilities of the input processing block, the output processing block and the computation block, equipped to support interleaved execution of multiple threads, includes a storage sub-block to store a thread switching structure that includes a current thread identifier identifying one of the multiple threads as a current thread to be executed, and a thread array including thread entries describing corresponding ones of the multiple threads.

27.   (Original) The media processor of claim 25, wherein at least a selected one of the facilities of the input processing block, the output processing block and the computation block, equipped to support interleaved execution of multiple threads, further includes an execution sub-block equipped to create a thread entry in the thread array for a thread as part of the execution of a create thread instruction spawning interleaved execution of the thread.

28.   (Original) The media processor of claim 25, wherein at least a selected one of the facilities of the input processing block, the output processing block and the computation block, equipped to support interleaved execution of multiple threads, further includes an execution sub-block equipped to reset an activeness indicator of a thread entry in the thread array for a thread from indicating an active state to indicating an inactive state as part of the execution of a thread termination instruction terminating execution of the thread.

29.   (Original) The media processor of claim 25, wherein at least a selected one of the facilities of the input processing block, the output processing block and the computation block, equipped to support interleaved execution of multiple threads, further includes an execution sub-block equipped to select a thread as a new current thread to be executed, updating a current thread identifier of the thread switching structure to identify the selected thread, and switching to

execute an instruction of the selected thread, as part of the execution of a thread execution switching instruction.

30.   (Currently amended) A system comprising:

a host processor;

first memory coupled to the host processor;

second memory;

a media processor coupled to the second memory and the host processor, the media processor having at least

a direct memory access unit to access media data, and

a plurality of signal processing units coupled to the direct memory access unit to

process the accessed media, at least a first of which signal processing units comprising

a set of registers,

an input processing block coupled to the set of registers, including an input interface, execution and thread management facilities equipped to support interleaved execution of multiple threads of instructions, the thread management facilities including a thread management sub-block equipped to maintain a thread switching structure including a current thread identifier to identify one of the plurality of threads as a thread to be executed, and a thread array of and create and add thread entries, one per thread, configured to describe the set of registers on which the corresponding threads depend, each thread entry to be created and added to the thread array by the thread management sub-block based on a create thread instruction to the multiple threads of instructions to a thread array within the thread switching structure, and wherein the thread management sub-block is further configured to select another thread of the plurality of threads to be executed based on a thread switching instruction, wherein the thread switching instruction may select a thread based on a fixed priority basis, a round robin basis, or a rotating priority basis; and

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an output processing block coupled to the set of registers, including an output

interface, execution and thread management facilities equipped to support

interleaved execution of multiple threads of instructions, the thread

management facilities including a thread management sub-block equipped

to maintain a thread switching structure and create and add thread entries

corresponding to the multiple threads of instructions to a thread array

within the thread switching structure;.

31.   (Original) The system of claim 30, wherein the first signal processing unit of the media processor further comprises a computation block coupled to the set of registers, including execution and thread management facilitates equipped to support interleaved execution of multiple threads of instructions, including instructions performing mathematical operations.

32.   (Original) The system of claim 31, wherein at least a selected one of the facilities of the input processing block, the output processing block and the computation block, equipped to support interleaved execution of multiple threads, includes a storage sub-block to store a thread switching structure that includes a current thread identifier identifying one of the multiple threads as a current thread to be executed, and a thread array including thread entries describing corresponding ones of the multiple threads.

33.   (Original) The system of claim 31, wherein at least a selected one of the facilities of the input processing block, the output processing block and the computation block, equipped to support interleaved execution of multiple threads, further includes an execution sub-block equipped to create a thread entry in the thread array for a thread as part of the execution of a create thread instruction spawning interleaved execution of the thread.   .

34.   (Original) The system of claim 31, wherein at least a selected one of the facilities of the input processing block, the output processing block and the computation block, equipped to support interleaved execution of multiple threads, further includes an execution sub-block equipped to reset an activeness indicator of a thread entry in the thread array for a thread from

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indicating an active state to indicating an inactive state as part of the execution of a thread termination instruction terminating execution of the thread.

35.   (Original) The system of claim 31, wherein at least a selected one of the facilities of the input processing block, the output processing block and the computation block, equipped to support interleaved execution of multiple threads, further includes an execution sub-block equipped to select a thread as a new current thread to be executed, updating a current thread identifier of the thread switching structure to identify the selected thread, and switching to execute an instruction of the selected thread, as part of the execution of a thread execution switching instruction.

36.   (Original) The system of claim 30, wherein the system is a selected one of a server, a palm sized personal digital assistant, a wireless mobile phone, a set-top box, an entertainment control console, a video recorder, or a video player.